

FIGURE 1 (PRIOR ART)

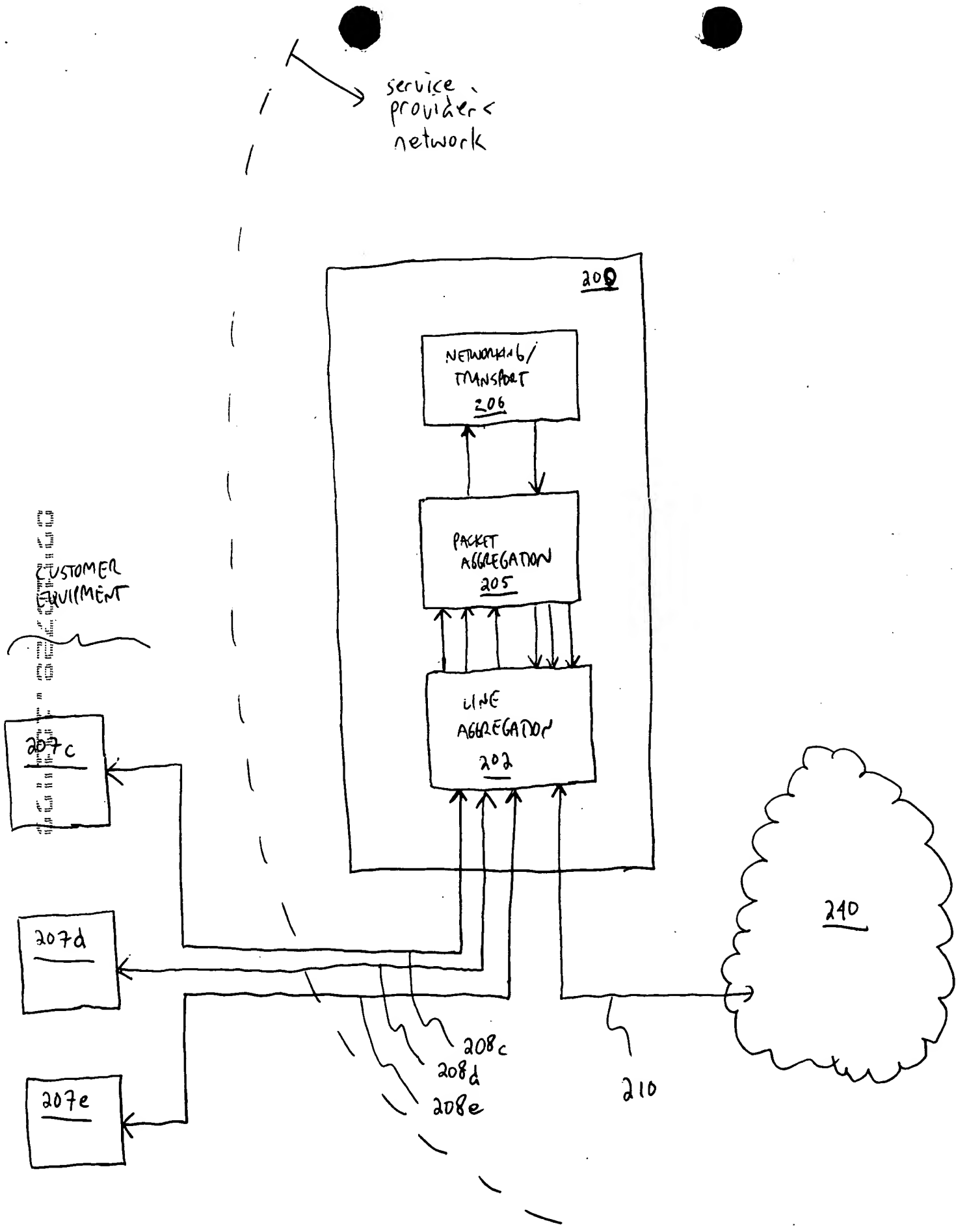


FIGURE 2A

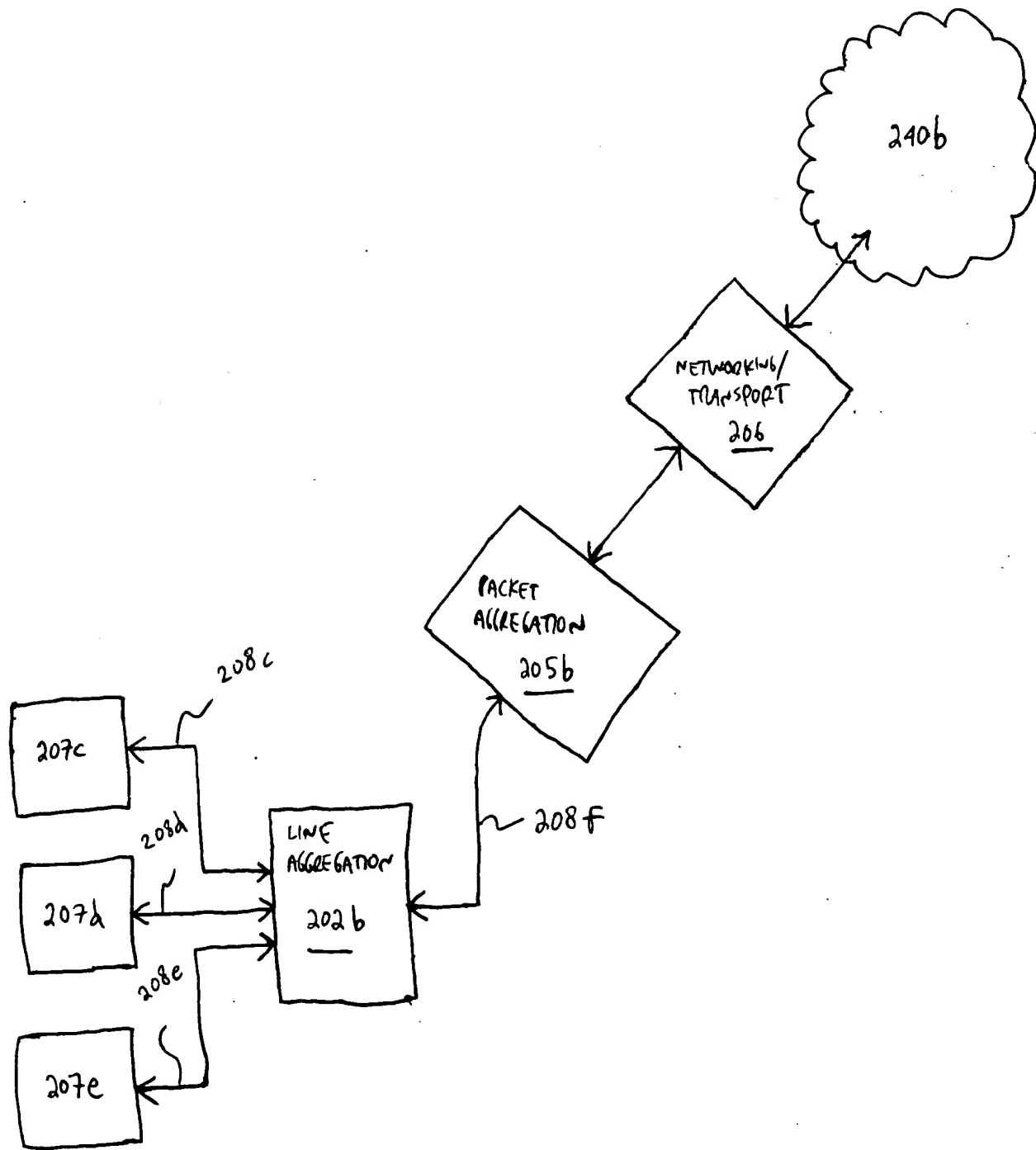


FIGURE 2b

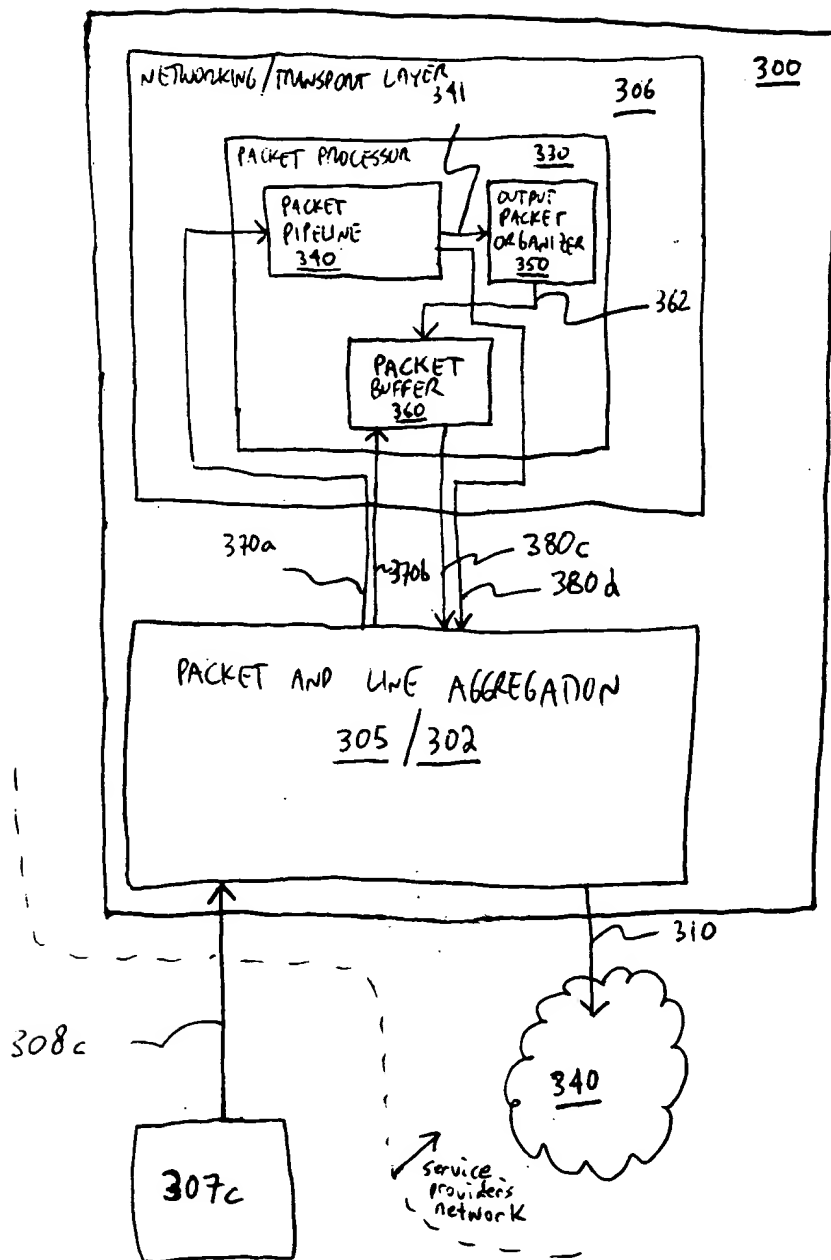


FIGURE 3A

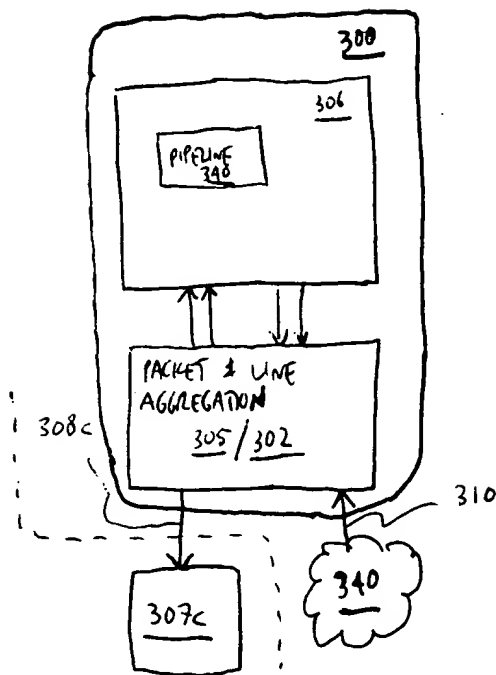


FIGURE 3B

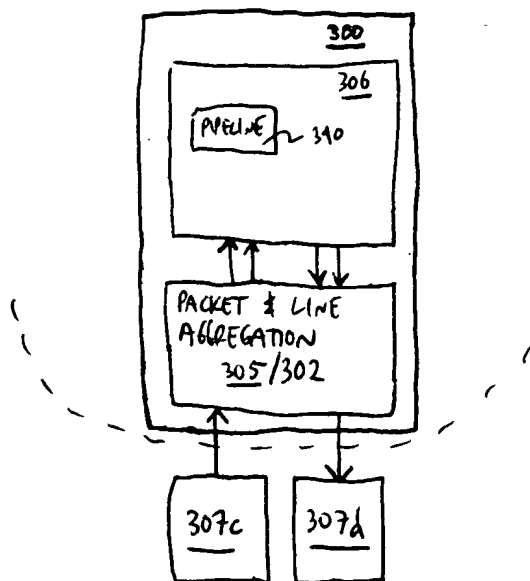


FIGURE 3C

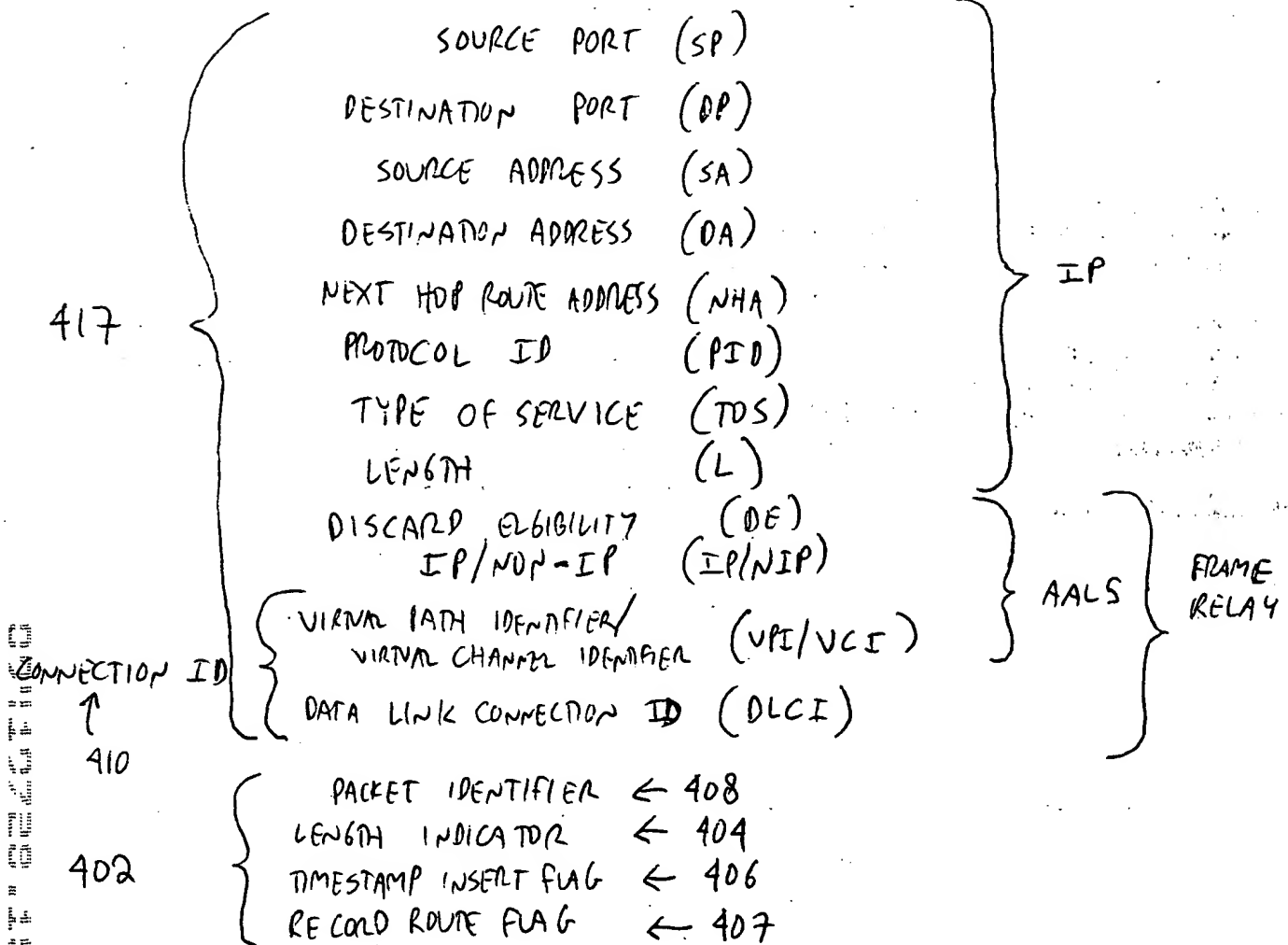


FIGURE 4

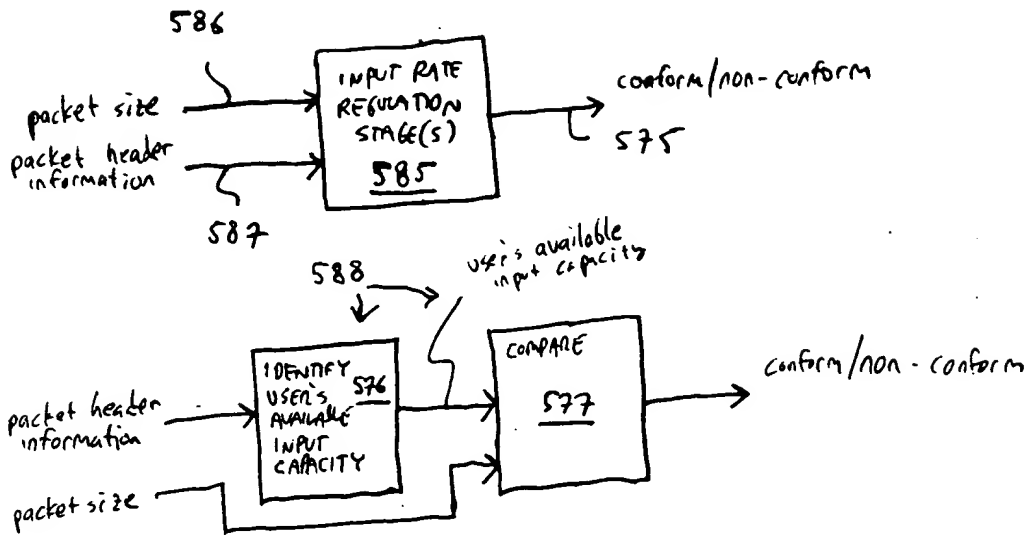


FIG. 5A

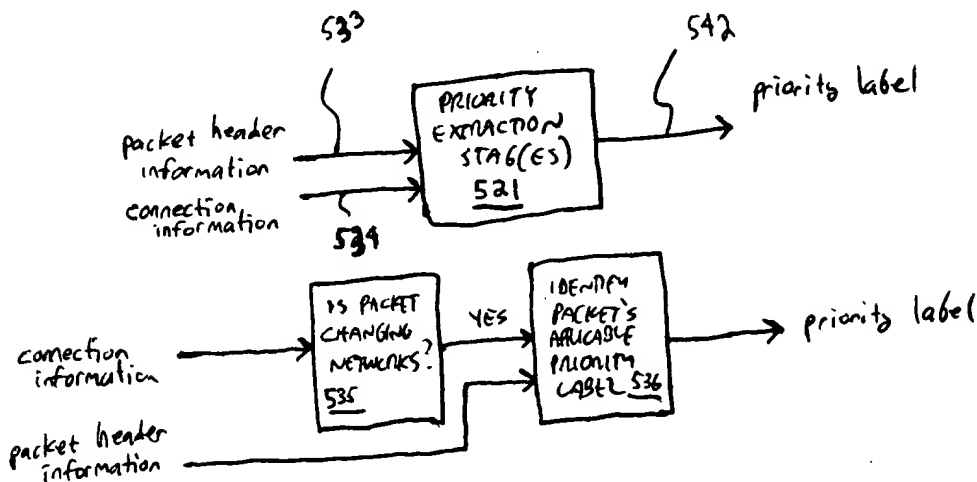


FIG. 5B

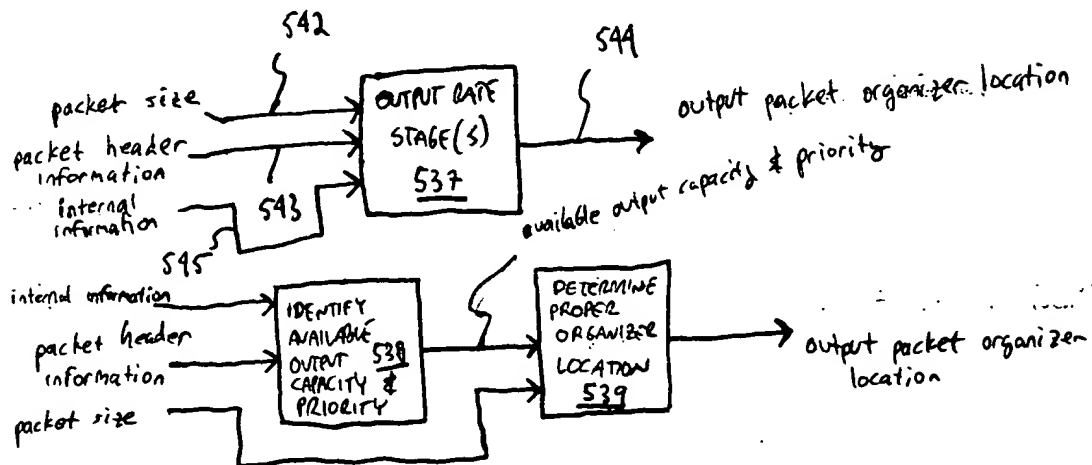


FIG. 5C

540

FIG. 5 is a block diagram of a network node 500, in accordance with one embodiment of the present invention. The network node 500 includes a control unit 510, a network interface 520, a memory unit 530, and a processing unit 540. The control unit 510 is connected to the network interface 520, the memory unit 530, and the processing unit 540. The network interface 520 is connected to a network 550. The memory unit 530 stores data and instructions. The processing unit 540 processes data and instructions. The network node 500 is configured to receive data from the network 550 and process the data according to the instructions stored in the memory unit 530.

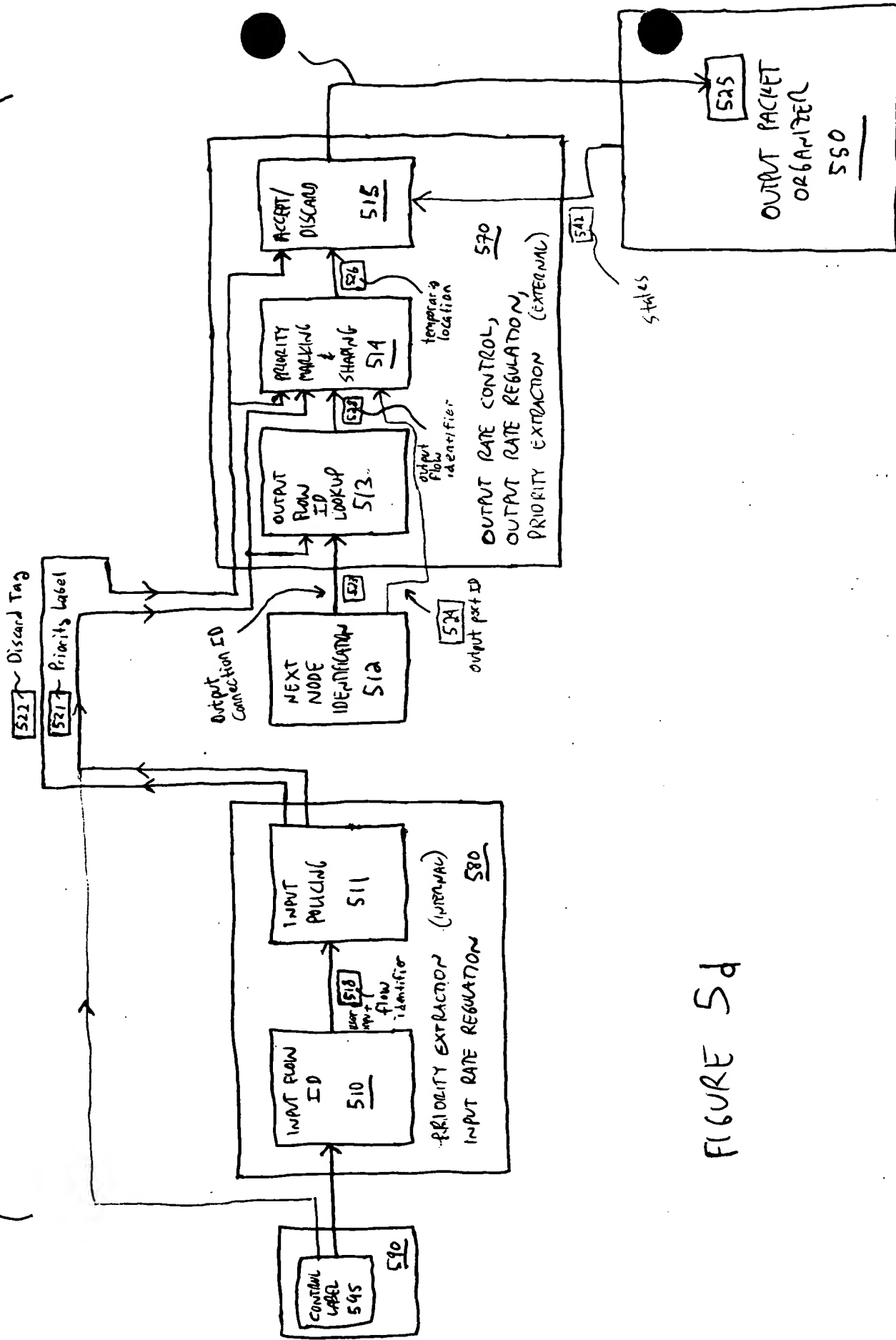


FIGURE 5d



FIG. 6A

INPUT FLOW ID STAGE	INPUT POLICING STAGE	NEXT NODE IDENTIFICATION STAGE	OUTPUT FLOW ID STAGE	PRIORITY MARKING AND SHAPING STAGE	ACCEPT/DISCARD STAGE
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X	X	X		X	X
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FIG. 6A

		X	X	X	X
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FIG. 6B

X	X	X	X	X	X
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FIG. 6C

		X		X	X
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FIG. 6D

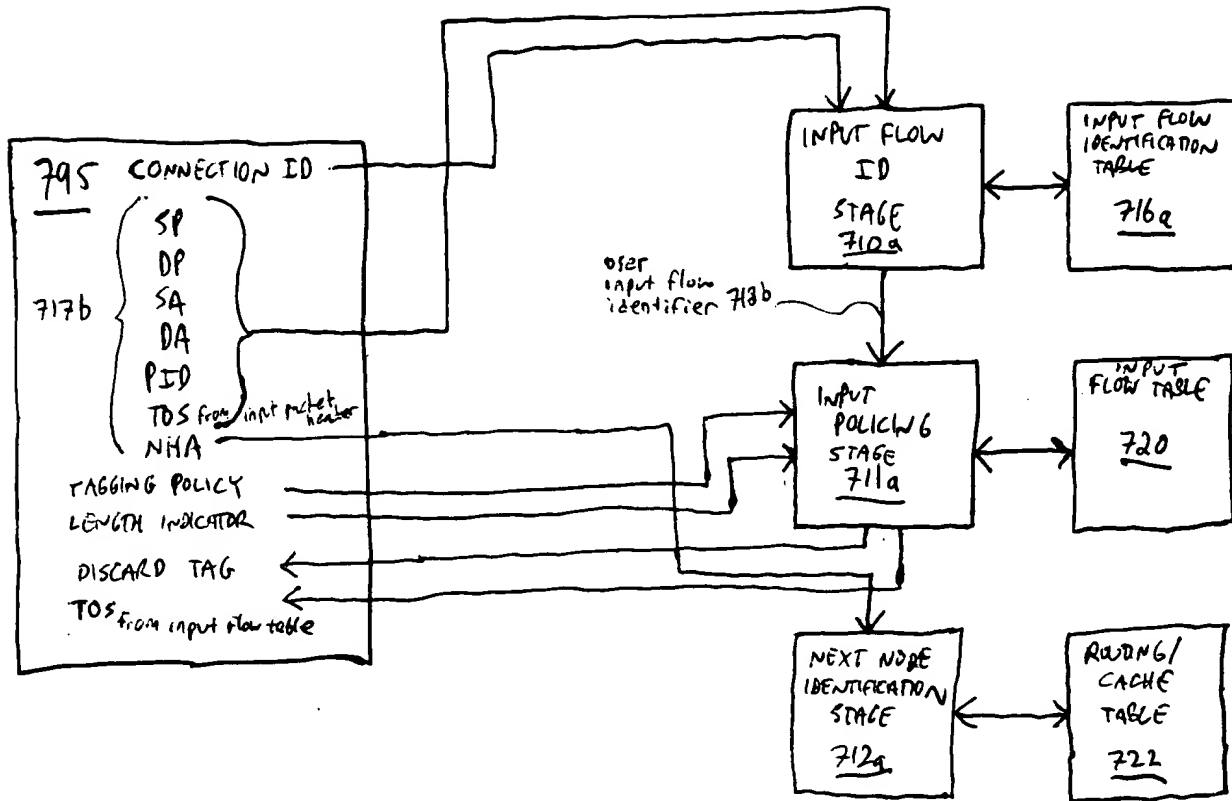


FIGURE 7A

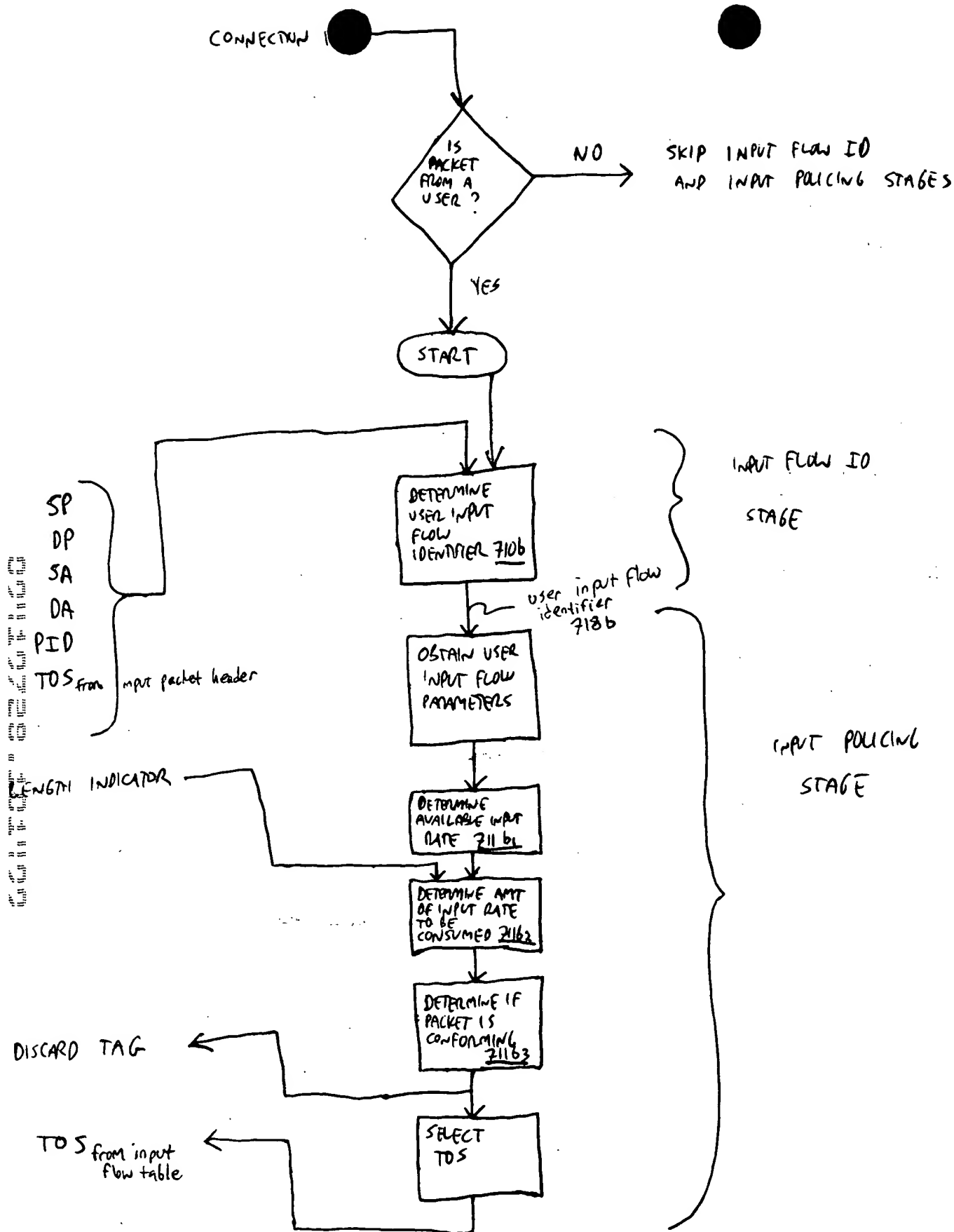


FIGURE 7B

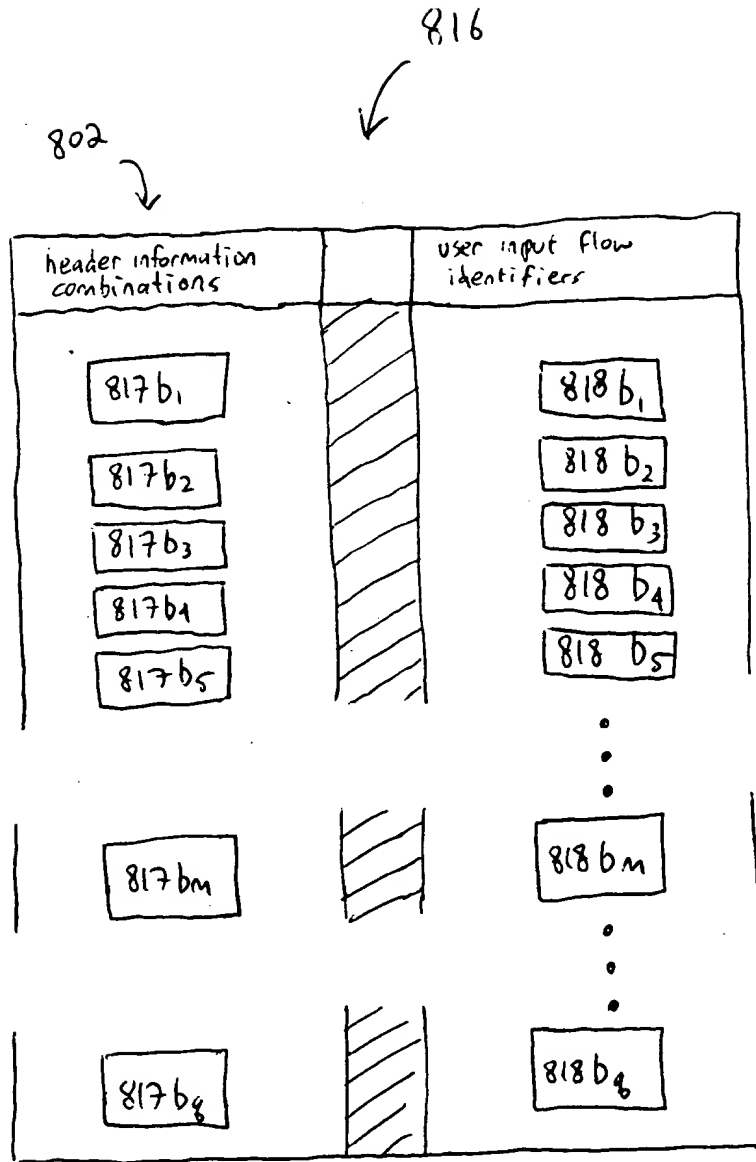
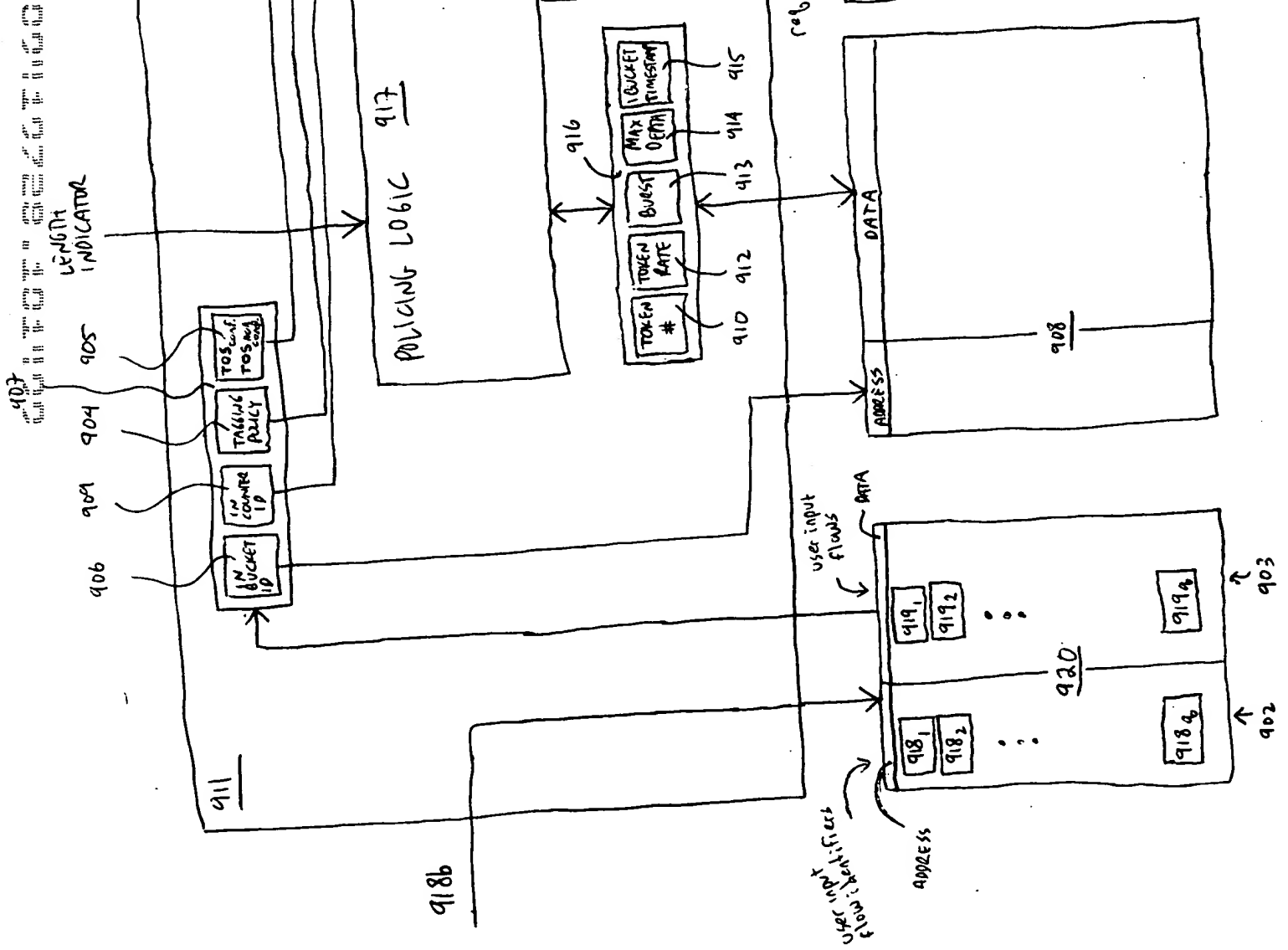


FIGURE 8

FIGURE 9



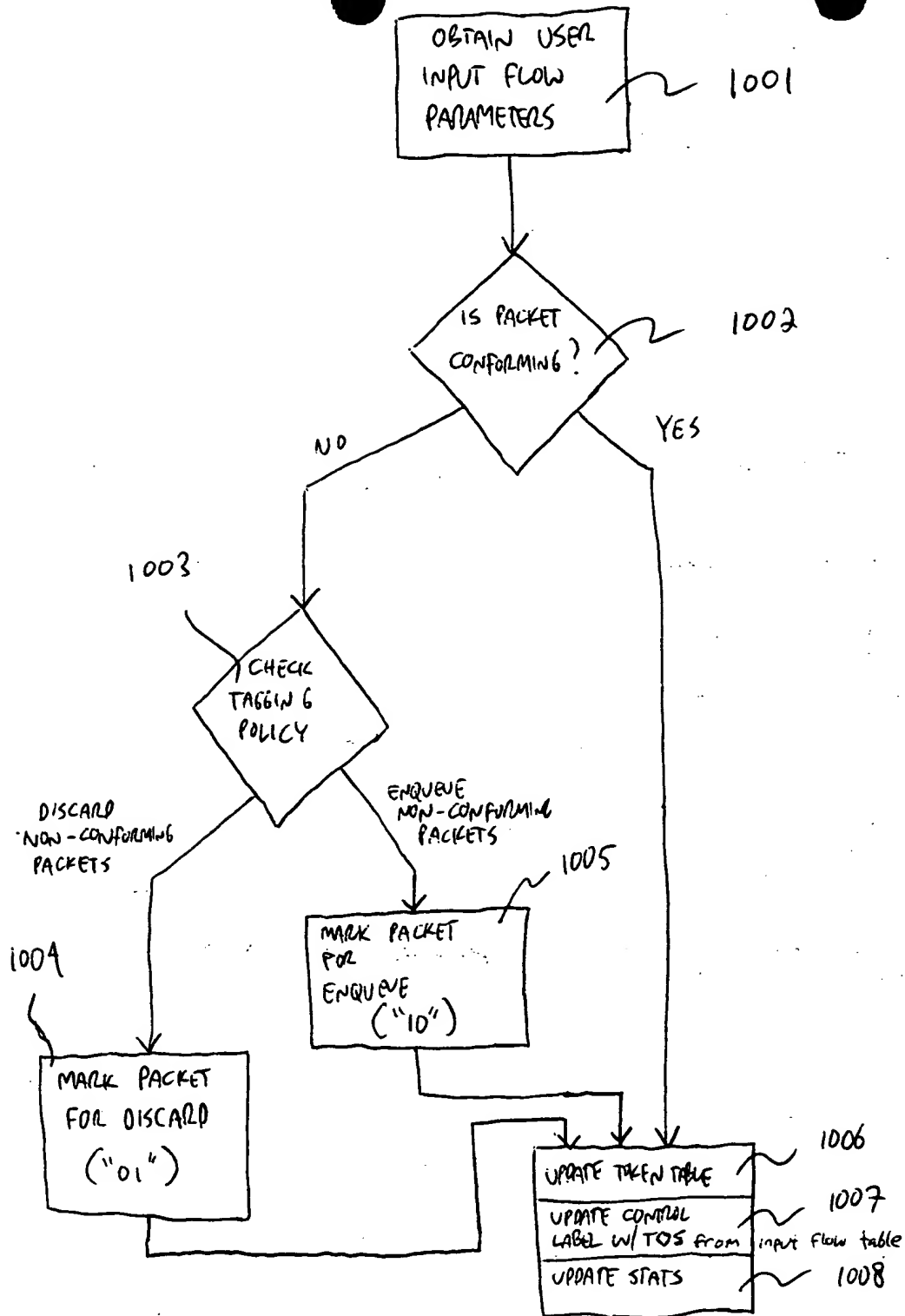


FIGURE 10



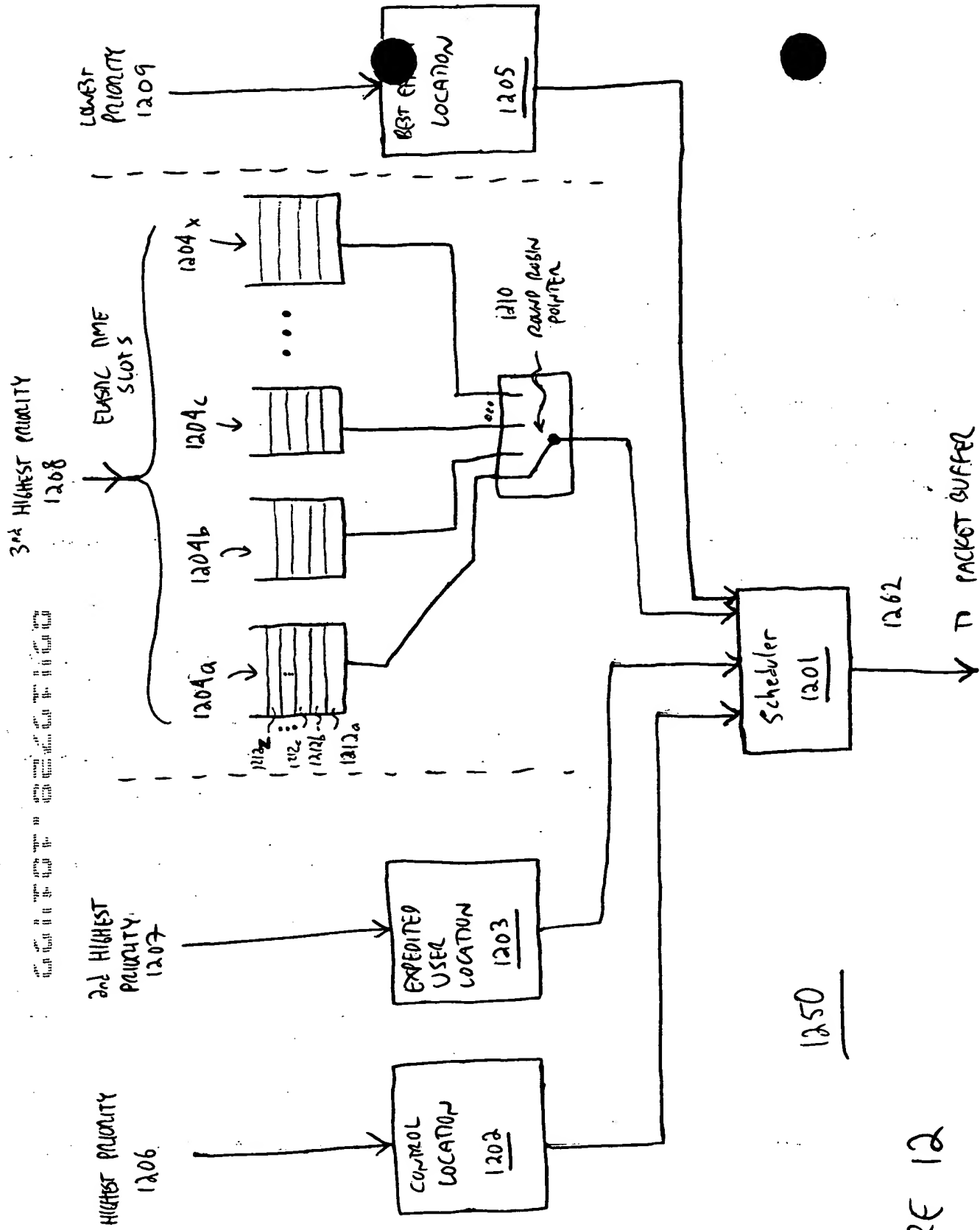


FIGURE 12



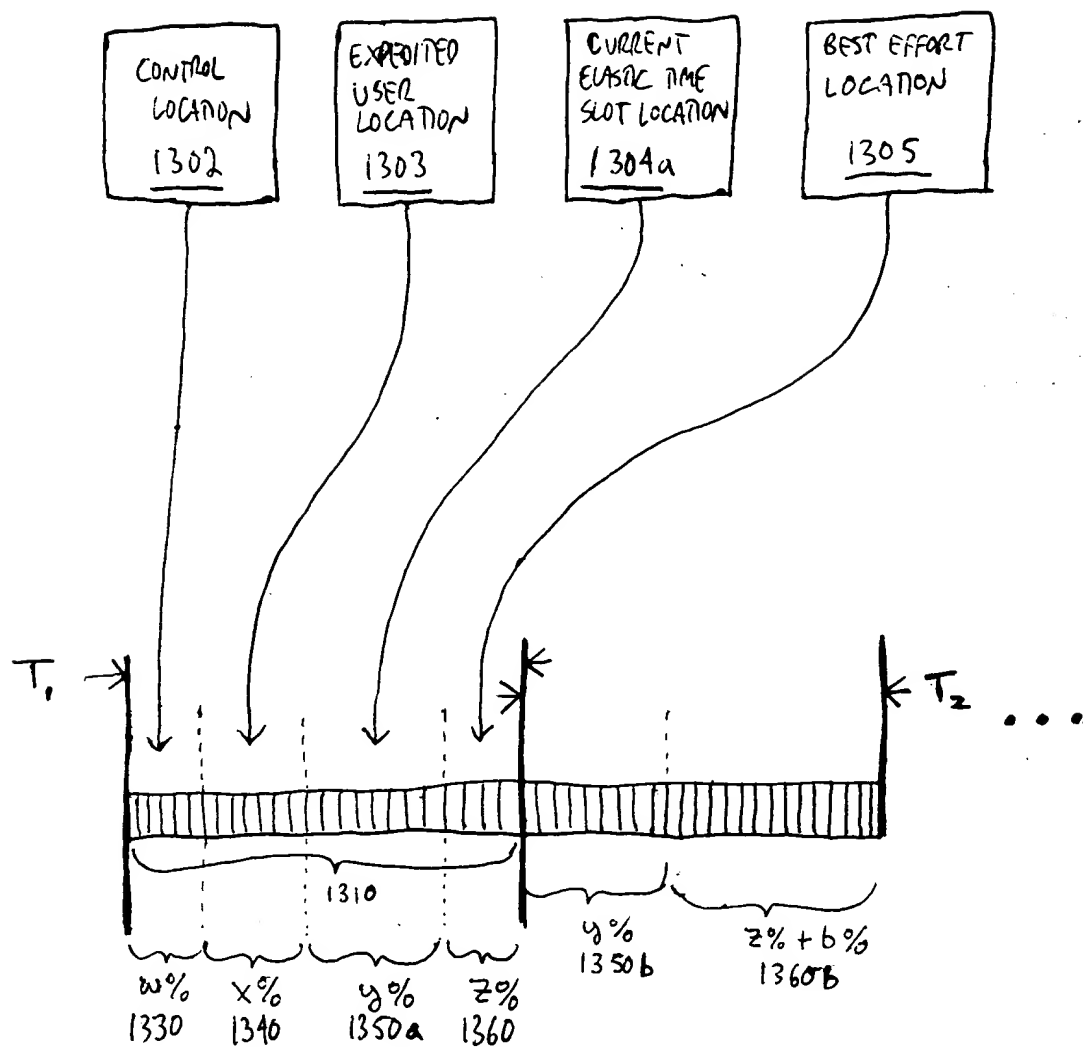


FIGURE 13

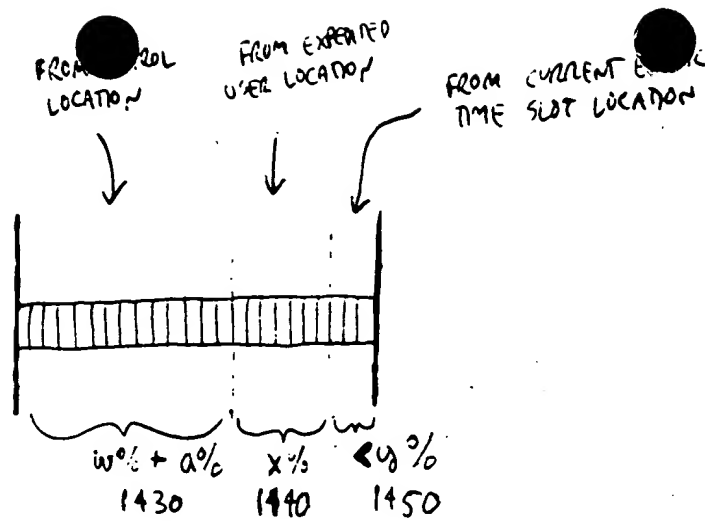


FIG. 14a

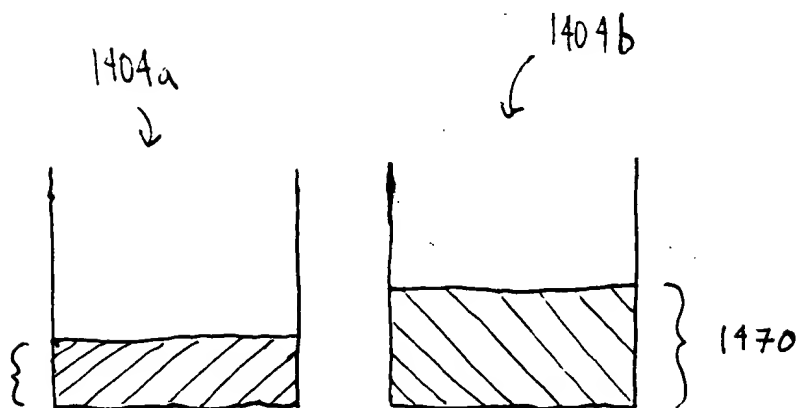


FIG. 14b

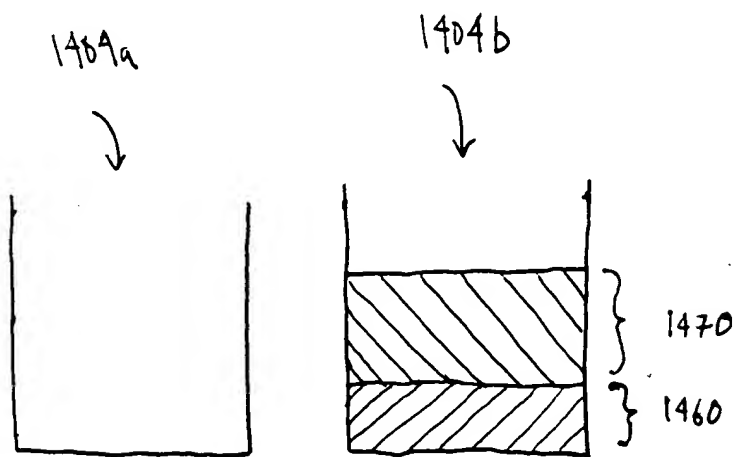


FIG. 14c

1500

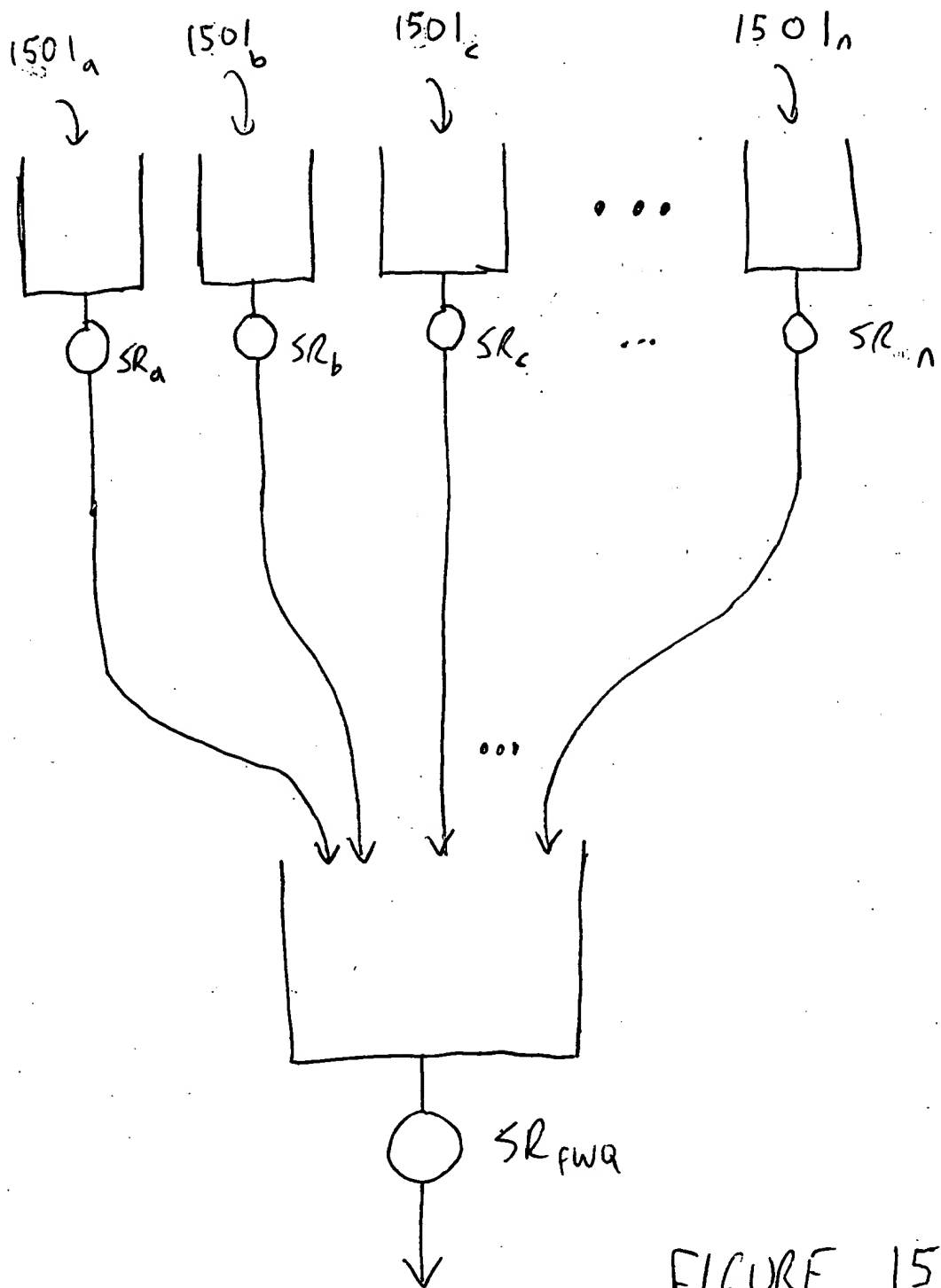


FIGURE 15

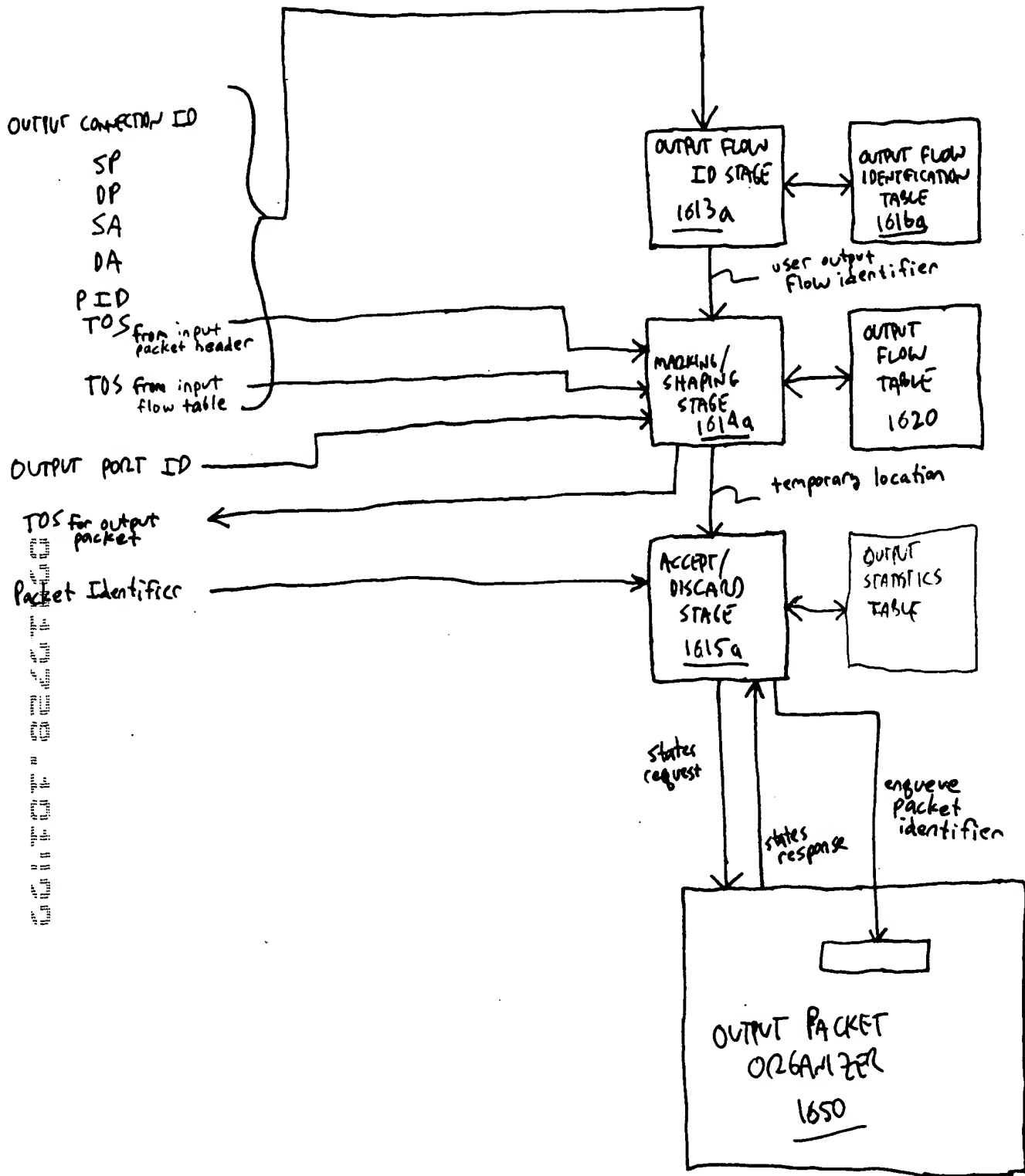


FIGURE 16<sub>a</sub>

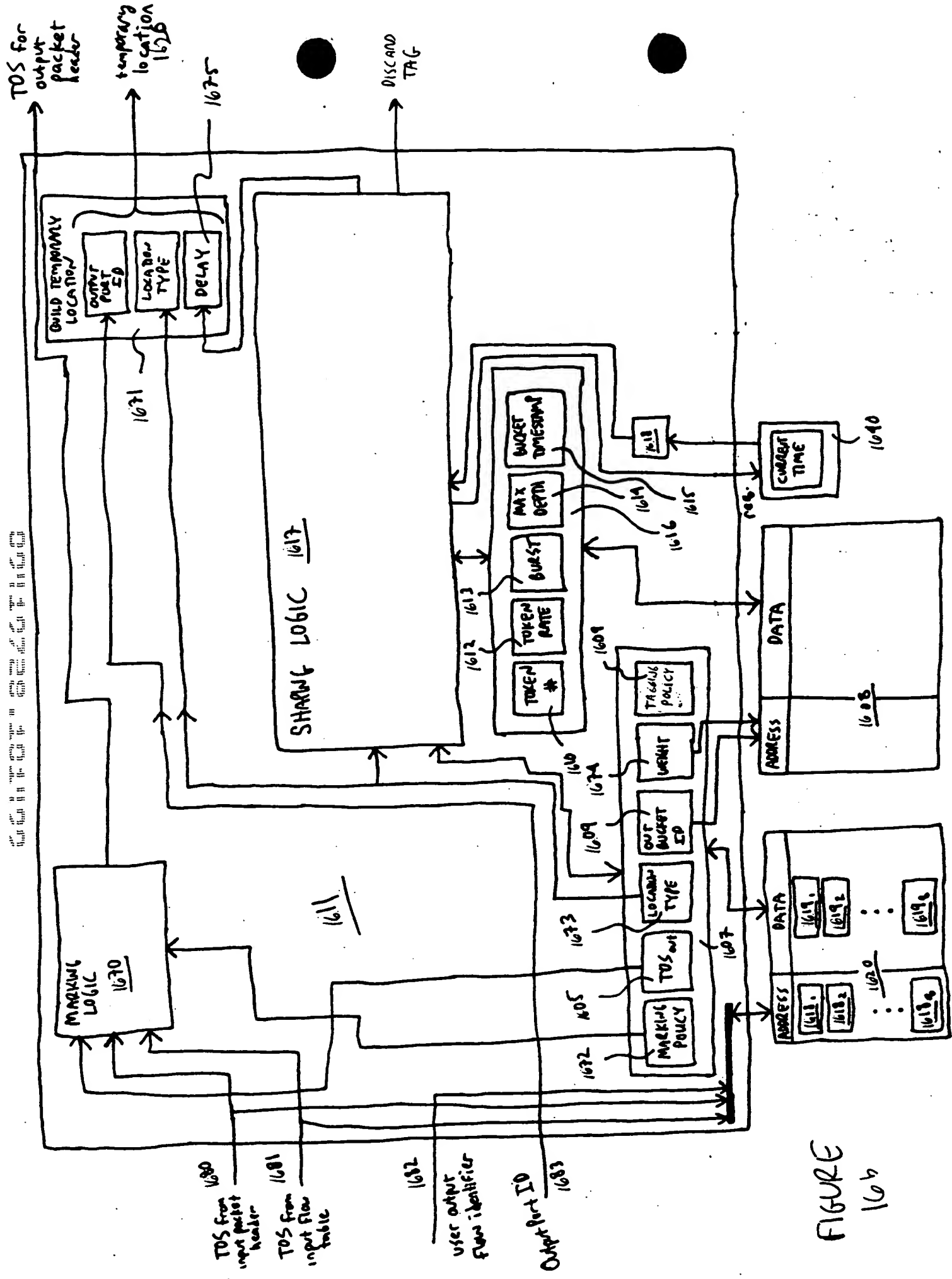


FIGURE 16b

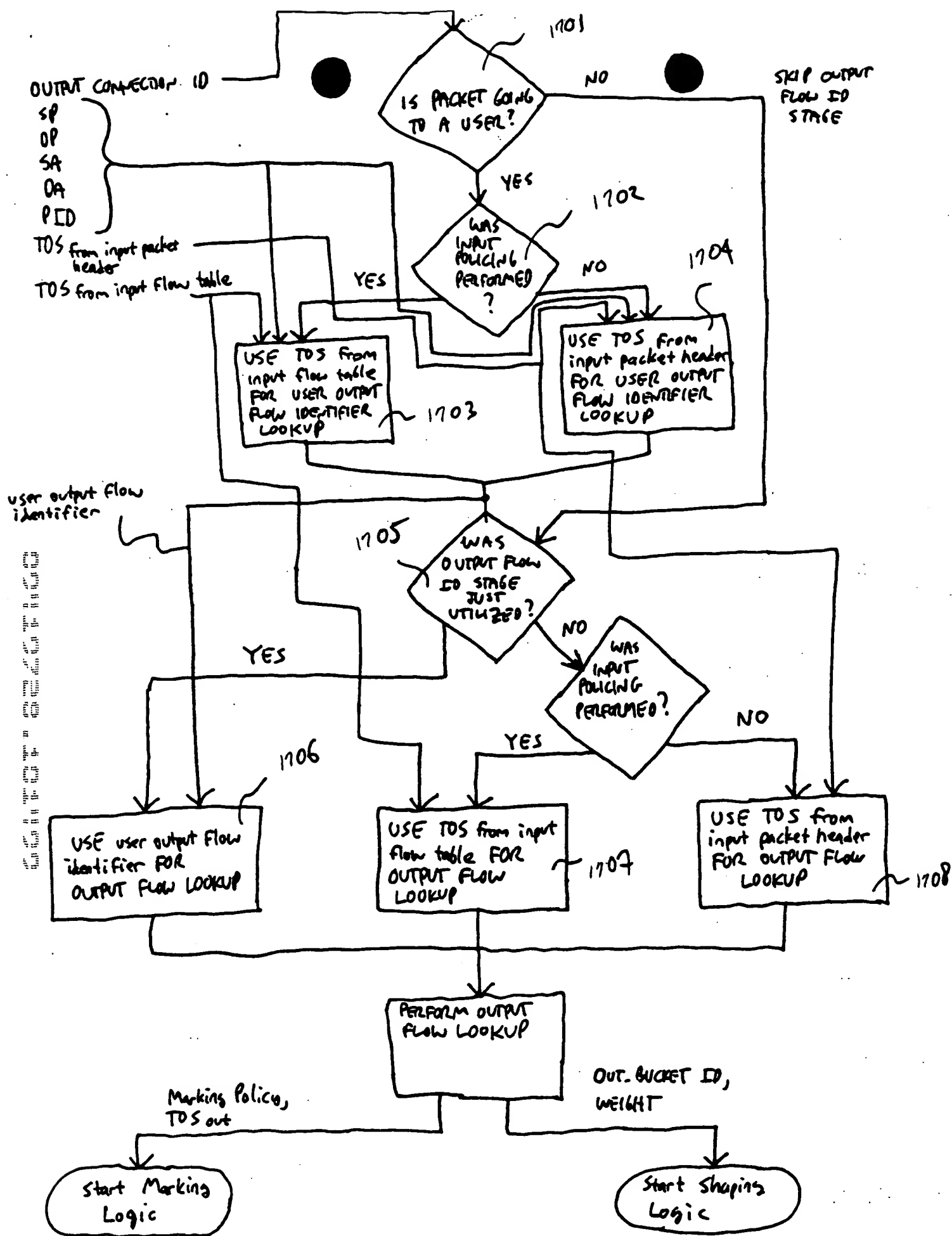


FIGURE 17a

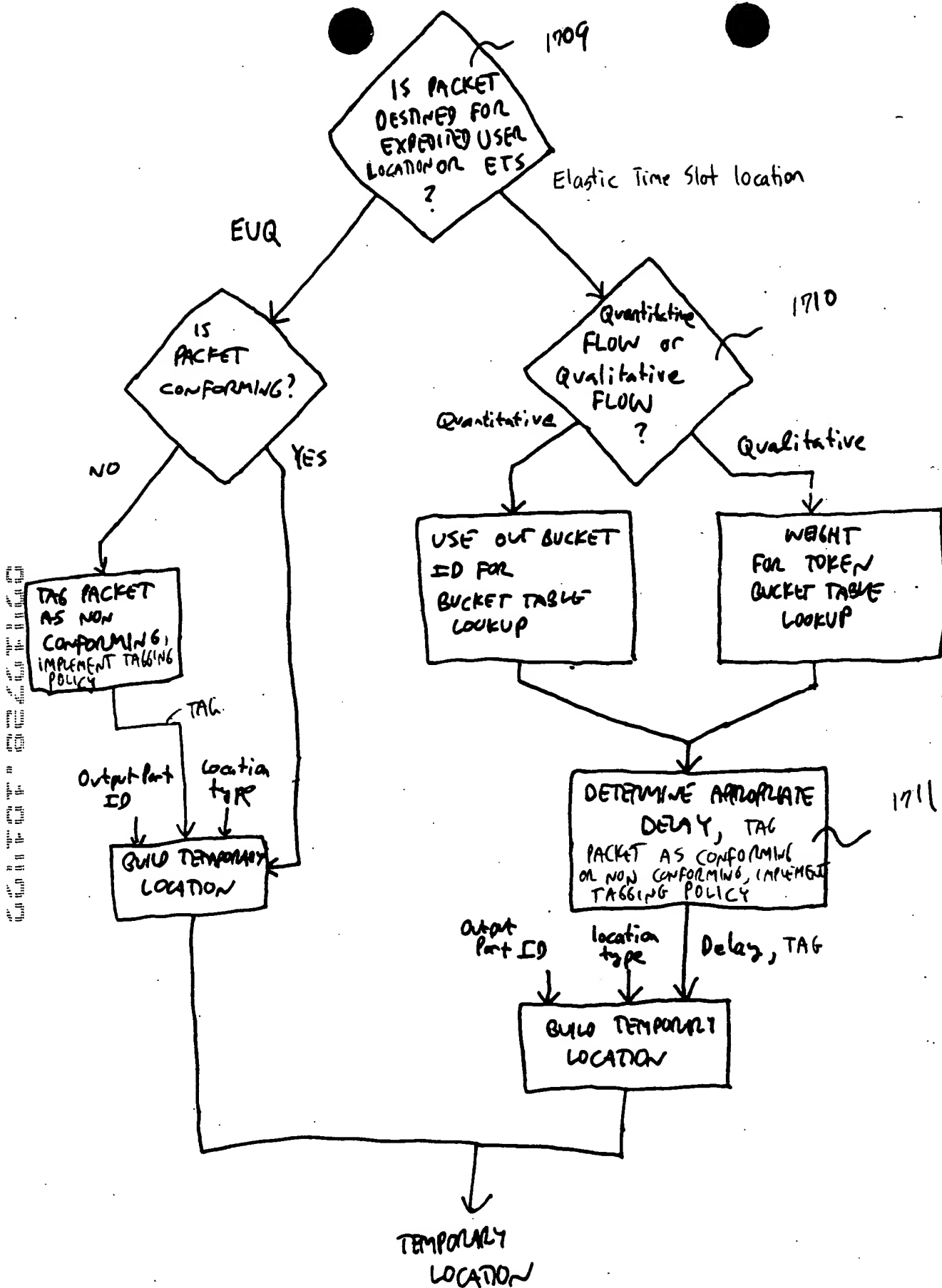


FIGURE 17b

## Marking Logic

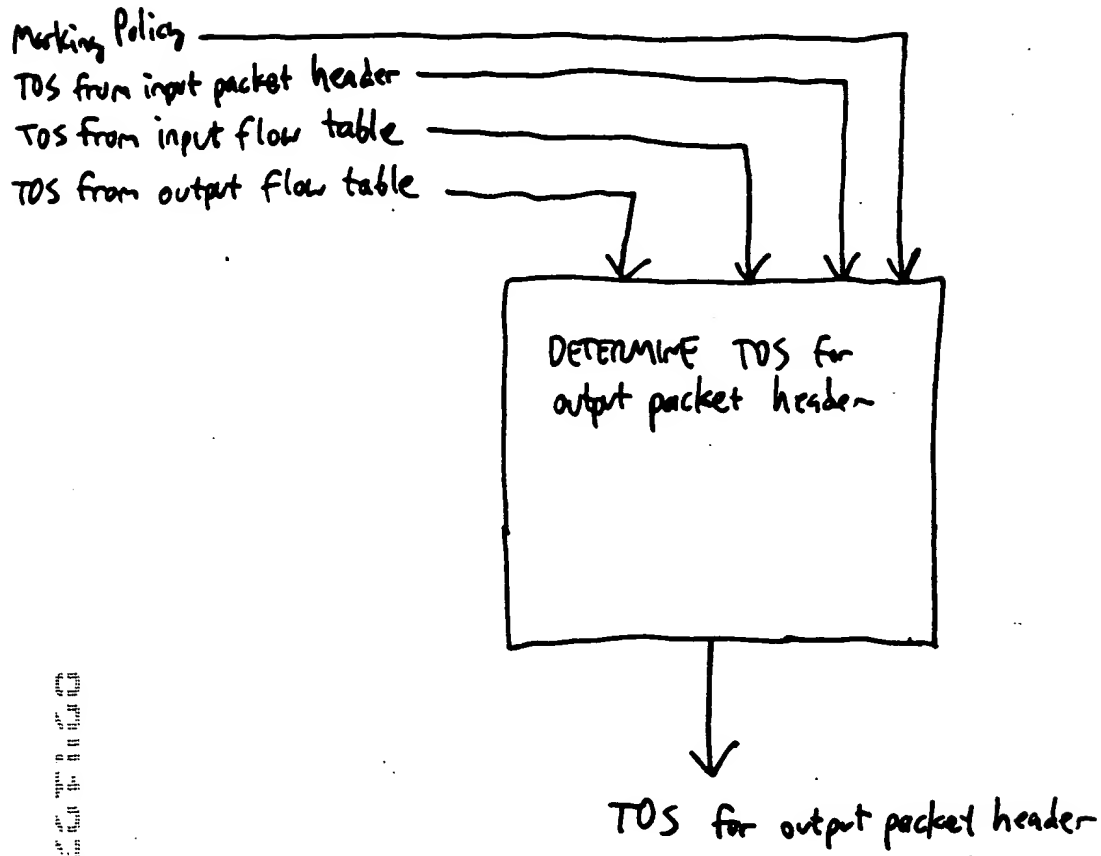


FIGURE 17c



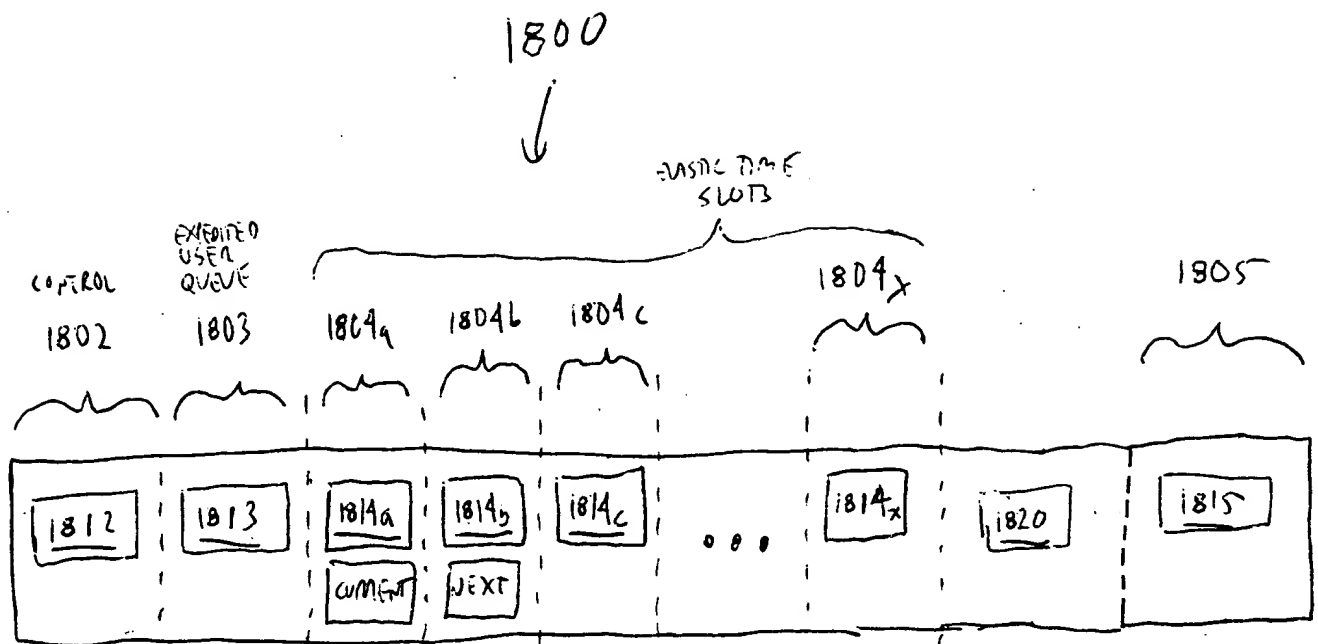


FIGURE 18